9. The device of claim 5 wherein said drain electrode is connected to said second semiconductor surface.

10. The device of claim 7 wherein said drain electrode is connected to said second semiconductor surface.

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11. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed identical hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface, the space between said hexagonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels;

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

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12. The device of claim 11 wherein said vertical common conduction region is disposed beneath said insulation layer means on said first surface.

Sub B2

13. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed identical polygonal base regions each having a second conductivity type formed in said lightly doped region and extending for a given depth beneath said first planar semiconductor surface, the space between said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

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a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

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a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels;

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

14. The device of claim 13 wherein said vertical common conduction region is disposed beneath said insulation layer means on said first surface.

15. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

Sub B3

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly

doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted; the space between adjacent ones of said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

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a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said

polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

16. The device of claim 15 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

17. The device of claim 15 wherein said drain electrode is connected to said second semiconductor surface.

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18. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a vertical common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

the surface of said common conduction region being continuous and uninterrupted and of said first conductivity type;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first

and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semi-conductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separate therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region;

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each of said at least first and second spaced base regions having identical polygonal configurations; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

19. The device of claim 18 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

20. The device of claim 18 wherein said drain electrode is connected to said second semiconductor surface.